Preparatory Questions (SHOULD BE ANSWERED BEFORE THE LAB!)

- Why simulation of semiconductor devices is important in semiconductor science and industry?

- Explain drain induced barrier lowering effect (DIBL).

- Explain channel length modulation effect (CLM).

- Explain body bias effect.

- Explain the avalanche breakdown.
Device Simulations lab A

Location: Bardeen (F302, IFM).
Download: http://www.ifm.liu.se/matephys/TFYA39/

I. Purpose of this Exercise

The development of nanoelectronic technologies and devices becomes more and more expensive and time consuming. On the one hand process steps and device structures are more complex and the equipment and production technologies ambitious, on the other hand theory and systems are more challenging due to the miniaturization of the nanoelectronic technology.

Rapid development of a CMOS (Complementary metal–oxide–semiconductor) technology would not be possible without extensive use of CAD (computer-aided design) simulation tools. CAD tools for simulation of device processing and electrical performance of devices in one, two or three dimensions are called TCAD (Technology CAD) tools. Throughout this laboratory exercise we will use a two-dimensional device simulator. The session consists of six projects. Each project explains some physical phenomenon affecting operation of a deep-submicron MOS transistor. Present state-of-the-art VLSI (Very-large-scale integration) technology employs devices with channel lengths ~0.18 μm. We will look at several effects present only in short channel devices and compare the simulations results with what would be expected from the original long-channel MOS transistor theory.

Because of complexity of the simulation suite, most of the files have been prepared for you. Try to gain a basic understanding of steps involved in the simulations and concentrate on analysis of the results. To sum up, the goal is two-fold:

1. Gain experience with TCAD simulation tools;
2. Learn about deep-submicron MOSFET operation.
II. Introduction to TCAD.

TCAD simulations are today an extremely important activity for the science and industry, since it makes it possible to explore technologies and concepts that do not yet exist in reality. TCAD simulations also provide information about the inner workings of devices, thus simplifying improvements on existing technologies. A complete TCAD simulation involves the following steps:

- Virtual fabrication of the device using a process simulator or a device editor;
- Creation of a mesh suitable for device simulation;
- Device simulation that solves the equations describing the device behavior;
- Post processing i.e., generation of figures and plots.

In this lab TCAD design flow is as follows: create device boundaries, doping profiles, and grids using MDraw, run the simulation using Dessis, and finally visualize the results using Tecplot and/or Inspect.

TCAD includes modules for meshing, process and device simulation, and visualization. All of them are invoked from the GENESISE window (Fig. 1). Some modules may be executed several times, giving rise to branches in the node tree. Many times, a simulation will automatically launch a proper visualization tool.

In more details about common TCAD simulation tools:

✓ MDraw

This first step of the TCAD tool-flow is intended to generate a structure that is suitable for device simulation. This means that the device structure should be described by its boundaries and materials. MDraw is used to graphically setup your device for simulation (Fig. 2). There are two operating environments, “boundary” and “doping”. You define the general shape of
your device and your contacts while in the “boundary” environment and then do everything else (doping and mesh) in the “doping” environment.

The generation of a device using a device editor is similar to making a drawing of the device; several basic geometrical elements are available like rectangles and lines. Each of these geometrical elements is also defined in terms of materials (aluminum, silicon, oxide, poly-silicon etc). Doping distributions are defined using analytical functions.

![Figure 2: Screenshot of MDraw after drawing a rectangle.](image)

- **Dessis**

  *Dessis* is the device simulation program itself, that carries all calculations. It numerically solves the drift-diffusion device equations over each of the mesh points using a finite difference method.

- **TecPlot**

  Visualization is very important for any scientific study because it aids in understanding concepts and results. For device simulation using TCAD tools, *TecPlot* (Fig. 3) is best for viewing 3D images of physical quantities throughout a device and for making cross-sections through a device and viewing quantities across them. *TecPlot* takes: *_mdr.grd* and *_des.dat* files as inputs and generates plots that can be exported into any of the most common graphic formats.
✓ **Inspect**

Another visualization tool - *Inspect* is used to plot one physical quantity versus another (Fig. 4). The most common use for Inspect is to plot current vs voltage.
III. TCAD Simulation Suite

For performing simulation you must login to a workstation by using Your LUKAS-ID as login name (abcde123) and own password. You need in UNIX Command Tool window initialize the simulation database and run the TCAD tool. This can be achieved by following steps:

*Right mouse click* on the desktop, in the pop out menu pick up *HOSTS* and choose *Terminal Console*

In appear UNIX window Command Tool; you can see all modules available by typing:

```
module avail
```

And you can add this course modules by typing:

```
module add ifm/tffy34
```

Now the module is added and you can start performing first lab just by typing:

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labA.ini
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IV. Project 1: Building a Simulation Mesh

In the first project, you will create a simulation mesh for a NMOS transistor with 0.18µm channel length. The final mesh will be used in all other projects.

In the GENESISE TCAD working window You will find six projects named Project1 to Project6. Choose project 1, this project becomes activated when you double click on it in Projects window. The project is ready to run. On the top, you can see all modules which are involved in the execution of Project1. There is only a single module called MDraw. Launch the project from the tool bar by clicking Run selected nodes( ) and then Run buttons. MDraw starts in the interactive mode by schematically drawing the NMOS outlook. Click on Materials on the top of the window. You should obtain a palette of materials. The pink color is used for Silicon and dark brown for oxide. On the top of the silicon rectangle, you can identify an oxide ‘hill’ with a rectangular hole in the middle, which is the transistor gate. Under the gate, there is a thin 40Å oxide layer. The red lines define contacts. There is a bulk contact on the bottom, source on the top to the left, drain on the top to the right and gate contact encircles the rectangular hole in the oxide ‘hill’. In the coming simulations we will completely neglect modeling of the polysilicon gate material. Change the view from Boundary to Doping (left-hand side lower corner of the window, see Fig. 2). Select Mesh→Build Mesh from the menu bar. A very course mesh is created. Each vertex of the mesh defines a point at which various functions, e.g. doping and carrier concentration, will be evaluated. Such mesh is very inaccurate and cannot be used for simulations. We have to define refinement regions, which tell the mesh generator where and how to improve the mesh. Remove the mesh by selecting Mesh→Delete Mesh. From the File menu, select Include Command File... and find file mdr_refine.cmd in the Project1 folder. Check the box Show Refinement on the left. A few white rectangles appear. Each rectangle defines a region of improved resolution. Try to create the mesh again Mesh→Build Mesh. The mesh is much better this time (Fig. 5). You can zoom in the region under the gate. The mesh is very fine in the channel region. To return to the default view, select View→Zoom Reset. Save the mesh File→Save Mesh→Dismiss. You can now quit MDraw by File→Quit. Do not save the user setup. Yellow color line should appear under MDraw icon indicating that project is complete successfully. Now you are ready for the second project.

Fig. 5. Doping concentration and simulation mesh of NMOS transistor.
V. Project 2: MOS Transistor Channel

Activate Project2 by repeating the steps outlined in Sect. IV. The results from Project1 have been linked to a device simulator Dessis, which reads the final mesh from MDraw. Therefore, you do not need to run MDraw anymore. The second module defines a parameter $V_{gs}$ with a default value equal to 0V. The third module is a visualization tool Tecplot, which displays the results from Dessis. In this project, you will study electron distribution in the NMOS transistor. The drain, source and bulk will be grounded, the voltage between the gate and the ground will be equal to $V_{gs}$. Dessis is a finite element solver which finds a coupled solution of Poisson and drift and diffusion equations for electrons and holes. The solution is found iteratively. Run the project from the tool bar. The simulation will be over when the yellow color appears. Now you need to visualize the results of this simulation, this can be done by using Tecplot tool by choosing Extensions→Run tecplot in main tool bar.

We are now ready to visualize the results. For obtaining simulation (transistor visualization) result of carrier concentrations you should import the files that are generated during the simulation. In your Tecplot window, go to the File menu and select Import... In the new window, select DF-ISE Loader and click on OK. In the new window that appears, select the following files and click Add:

```
device.grd
n2_des.dat
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These are the two necessary input data files. The first is the grid file output from MDraw and the second is the output file from Dessis.

Now your simulation results are visualized by Tecplot. You need to get electron ($eDensity$) and hole density ($hDensity$) in channel region, but the channel region is too narrow. Choose Zoom tool and zoom in channel region. For being precise You can read data by using Tool to probe the data→tool details... and in this tool choosing: Probe At... by entering exact coordinates on device. Highlight $eDensity$ and $hDensity$ on the list. Estimate electron and hole concentration in the channel region and fill these values in Table 1.

Quit Tecplot without saving layout. Electric field in the depletion regions has the same effect as a positive gate bias on the gate. It supports creation of a channel and locally reduces the threshold voltage. This effect is called drain-induced barrier lowering (DIBL). You will learn more about DIBL in Project3. In the GENESE menu bar, press Project→Cleanup. Change the value of $V_{gs}$ (see Table 1). Run Project2 again and in the same way as before, find carrier concentrations in the channel region. Fill in Table 1 completely.

Table 1: Carrier concentration

<table>
<thead>
<tr>
<th>$V_{gs}$ [V]</th>
<th>Electrons [cm$^{-3}$]</th>
<th>Holes [cm$^{-3}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
How changes carrier concentration with gate voltage?

VI. Project 3: Threshold Voltage

In this project you will learn how to estimate MOSFET threshold voltage and how it is affected by DIBL.

Activate Project3. If you look in the Family tree you will notice a new block defining voltage between drain and source $V_{ds}$. According to the long-channel theory, drain current is independent of drain voltage when a transistor operates in the saturation region ($V_{GS}-V_T < V_{DS}$). In the subthreshold region, this condition is satisfied, but you will see some deviation from the long channel theory in the simulations. For each given value of $V_{ds}$, Dessis performs a sweep of gate voltage from 0V to 1.8V. From one simulation run, you will obtain a curve $I_d(V_{GS})$ for a given value of $V_{ds}$. The simulation will be run for $Vds$ equal 0.5V and 1.8V, so you should finally obtain two curves $I_d(V_{GS})$.

Run the project. The simulation takes about 4 minutes and you will get an Inspect window. Change the Y axis scale to logarithmic. Explain shortly why the curves do not match even for very low gate voltage. You may want to take another look at the discussion in Project 3.

Change the Y axis scale back to linear and estimate the threshold voltage of the transistor. According to the long-channel theory, $I_d(V_{GS})$ should be a parabola for $V_{GS}$ between $V_T$ and $V_{DS} + V_T$. 
VII. Project 4: Transistor Characteristics

In Project3 (Sect. VI), you looked at the drain current dependence on gate voltage for a fixed drain voltage. In this project, you will plot drain current dependence on drain voltage and keep gate voltage constant. Activate Project4.

Open the Tool Flow window and you will find that the parameter has been renamed to $V_{gs}$. In the Family tree window you can see that the execution tree has four branches after Dessis. Run the project from the tool bar. It will take ~5 minutes before an Inspect window pops up. Read appropriate values from the graphs and fill in Table 2. Use threshold voltage $V_T$ from Project3.

Table 2: Drain current in saturation, $V_{DS}=1.8\text{V}$

<table>
<thead>
<tr>
<th>$V_{GS} [\text{V}]$</th>
<th>$I_D [\text{A}/\mu\text{m}]$</th>
<th>$I_D/(V_{GS}-V_T)^2 [\text{A}/\mu\text{mV}^2]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
<td></td>
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</tbody>
</table>

According to the long-channel theory, $I_D\sim(V_{GS}-V_T)^2$ in the saturation region. Comment on the results in Table 2.

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Explain why $I_D(V_{DS})$ increases even in the saturation region, while in the ideal case it was supposed to be constant.

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VIII. Project 5: Body Effect

Project 5 is very similar to Project 3, where you obtain $I_D(V_{GS})$ curves for various drain voltages $V_{DS}$. How does the bulk (also called body or substrate) bias affect the threshold voltage of the transistor?

IX. Project 6: MOSFET Breakdown

In this project you will learn what happens with a transistor, if you increase drain voltage beyond the limit of safe operation. Activate Project 6, but before running it first do: Project → unlock. This simulation takes approximately 10 minutes. Fig. 6 shows schematics of the simulated circuit.

![Fig. 6. Circuit for breakdown simulation.](image)

Gate, source and bulk of the transistor are grounded. A protection resistor is connected between the drain and the voltage supply to limit the current in the breakdown region. The breakdown characteristics in the Inspect window shows drain current dependence on the internal drain voltage.

You can see that the curve does not resemble breakdown characteristics of a diode. It has a region with negative differential resistance that can be found in the breakdown characteristics of a bipolar transistor. You can see the transistor at the end of simulation, when the largest current flows through the drain. Explain simulation results.
Notes: